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L6 same repair$	36

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Search History

DATE: Thursday, May 27, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L7	L6 same repair$	36	L7
L6	unused adj1 redundant	101	L6
L5	unsed adj1 redundant	0	L5
L4	l1 same redundant	5	L4
L3	l1 same redundant same row	2	L3
L2	L1 and bisr	11	L2
L1	field adj1 repair$	1143	L1

END OF SEARCH HISTORY

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Search: L20

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Search History

DATE: Thursday, May 27, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L20	L15 and l1	5	L20
L19	L18 and l1	0	L19
L18	L15 and bisr	4	L18
L17	L14 and l11	1	L17
L16	L15 and l11	0	L16
L15	system-on-a-chip	366	L15
L14	system near3 chip	15566	L14
L13	L11 and redundant	23	L13
L12	L11 and l4	0	L12
L11	L10 and l3	499	L11
L10	soc	115682	L10
L9	L1 same bisr	4	L9
L8	L6 same l1	3	L8
L7	L6 same redundant	440	L7

L6	L4 same repair$	440	L6
L5	L4 same l3	4	L5
L4	redundant same row same column	2114	L4
L3	L2 same l1	3414	L3
L2	test$	836078	L2
L1	retest$	5062	L1

END OF SEARCH HISTORY

L7: Entry 10 of 36 File: USPT Jul 1, 2003

DOCUMENT-IDENTIFIER: US 6586823 B2
TITLE: Semiconductor device that can have a defective bit found during or after packaging process repaired

Detailed Description Text (42):
In other words, repair can be effected by carrying out replacement with an unused redundant cell in a semiconductor memory chip by means of a replacement information storage unit 10 provided in the package to store replacement information, or by adding replacement information to change the address corresponding to replacement for the redundant memory cell row and redundant memory cell column already used. It is therefore possible to repair a defect even after assembly to improve the yield of the multichip module.

L5: Entry 2 of 4 File: USPT Nov 10, 1998

DOCUMENT-IDENTIFIER: US 5835431 A
TITLE: Method and apparatus for wafer test of redundant circuitry

Detailed Description Text (15):
One skilled in the art will appreciate that wafer testing of a memory array within a microprocessor, and reporting of defects in the memory array to a manufacturer is known in the art. In addition, removal of the wafer from a tester, to blow a fuse to disable a defective row/column, and re-testing of the memory array to determine whether defects exist in a redundant row/column is also known. What will now be shown is a method and apparatus according to the present invention that allows a redundant row/column to be tested during the first wafer test, without having to blow a fuse, and retest the wafer.

L20: Entry 4 of 5 File: USPT Aug 10, 1999

DOCUMENT-IDENTIFIER: US 5936876 A
TITLE: Semiconductor integrated circuit core probing for failure analysis

Brief Summary Text (6):
Automated probe systems and functional testers are known for testing ICs at wafer sort, i.e. before packaging. Typically, an entire silicon wafer with perhaps hundreds of integrated circuits formed on it is functionally tested before the wafer is cut into individual chips or dies for packaging. At this stage, the integrated circuits are tested, one at a time, using a probe machine. The probe machine handles the wafers and positions a "probe card" contacting the particular circuit under test. The probe card has a number of individual probes--typically several hundred in the context of large-scale integrated circuits arranged--for contacting corresponding bonding pads along the peripheral edges of the chip. The probe card provides electrical connection of the chip to an automatic tester machine which measures various I/O ac and dc properties, and otherwise "exercises" the chip to confirm functionality. "Bad" parts are rejected while good ones are packaged (and sometimes retested) and shipped to customers. Wafer sorting systems of the type just described are not used for failure analysis, however, or are used only in limited ways, because failure analysis often requires testing and measurements at internal locations on the die that are not connected to bonding pads.

Brief Summary Text (7):
This problem can be illustrated using embedded memory in an ASIC as an example. Recent advances in semiconductor technology allow the use of increasingly large blocks of memory, such as synchronous RAM or asynchronous RAM cores in ASIC. It is commonplace today for a "system-on-a-chip" to include several megabytes of embedded RAM. Consequently, wafer testing of the ASIC during manufacture must include automatic testing of embedded memories. However, testing of embedded memory blocks in ASIC is very challenging for several reasons. First, a large number of patterns are required for a comprehensive memory test; and the number of patterns grows exponentially with the increasing size of memory. Moreover, accessing memory to apply the test and then to observe the response is a major challenge when the memory is buried deep in the logic.

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L5: Entry 4 of 4 File: USPT Jul 3, 1990

DOCUMENT-IDENTIFIER: US 4939694 A
TITLE: Defect tolerant self-testing self-repairing memory system

Brief Summary Text (5):
After completion of the wafer probe tests, a laser repair procedure replaces defective memory cells with redundant rows and columns. If the number or placement of redundant rows and columns is not sufficient to repair the defective memory cells, the die is discarded. After completion of laser repair, the prior art retests the wafer. All failing die must be discarded because the prior-art procedures have no way to repair them.

L8: Entry 1 of 3 File: USPT Feb 3, 2004

DOCUMENT-IDENTIFIER: US 6687862 B1
TITLE: Apparatus and method for fast memory fault analysis

Brief Summary Text (4):
Memory such as DRAM stores bits organized in a grid of rows and columns where each bit is a binary digit. To increase yield of usable chips, DRAMs are typically manufactured containing a number of redundant, or spare, rows, redundant columns, or both. When a faulty bit is found, the row or the column containing the faulty bit is replaced by one of the redundant rows or redundant columns. A DRAM is repairable when the number of redundant rows is greater than or equal to the number of rows requiring replacement by a redundant row and the number of redundant columns is greater than or equal to the number of columns requiring replacement by a redundant column. If this condition is not met, then the DRAM is not repairable. Determining repairability depends on determining defect clustering from the raw data stream of addresses (column and row) and failed data bits in each word. If a DRAM can be repaired, the DRAM is then repaired through laser zapping to activate good columns or rows and retested to determine usability. The process of determining repairability, offline repair, and retesting requires additional testing time.

L8: Entry 2 of 3 File: USPT Nov 10, 1998

DOCUMENT-IDENTIFIER: US 5835431 A
TITLE: Method and apparatus for wafer test of redundant circuitry

Detailed Description Text (28):
If the memory array is not repairable, a similar report is made. This report, however, allows the manufacturer to scrap the chip without having to incur the expenses of blowing fuses to enable redundant rows/columns, and retesting the memory array to determine whether defects exist in the redundant rows/columns.

L9: Entry 1 of 4 File: USPT Apr 27, 2004

DOCUMENT-IDENTIFIER: US 6728910 B1
TITLE: Memory testing for built-in self-repair system

Abstract Text (1):
A method is presented for self-test and self-repair of a semiconductor memory device. A single built-in self-test (BIST) engine with an extended address range is used to test the entirety of memory (i.e., both redundant and accessible memory portions) as a single array, preferably using a checkerboard bit pattern. An embodiment of the method comprises two stages. In the first stage, faulty rows in each memory portion are identified and their addresses recorded. Known-bad rows in accessible memory are then replaced by known-good redundant rows, and the resulting repaired memory is retested in a second stage. During the second stage, repair of the accessible memory portion is verified, while defects among the redundant portion are ignored. Compared to existing methods, the new method is believed to simplify the interface between the BIST and the built-in self-repair (BISR) circuitry, reduce the overall size of test and repair circuitry, and provide improved test coverage.

Brief Summary Text (9):
A typical BIST/BISR method employs two BIST stages (also referred to herein as BIST "runs"). In the first stage, the accessible memory is tested row-by-row until a defect is encountered. The row containing the defect is then replaced by the first available redundant row and retested. This process continues until all of the accessible memory has been tested, or until there are no more redundant rows to use as replacements. In the first case, a second BIST run is performed, verifying all of the accessible memory. In the second case, the device is flagged as non-repairable. The two-stage method suffers from several drawbacks, among them the fact that it may overlook adjacent row interaction defects in the memory. Since the method tests accessible memory and redundant memory separately, it cannot detect interaction between adjacent accessible and redundant rows. A further disadvantage of the conventional two-stage method is that the total test time is not predictable. The duration of the test is dependent on the number of bad accessible memory rows, each of which has to be replaced and retested. Since there is no way to know the test time in advance, precise test scheduling during production is impossible.

Brief Summary Text (16):
The method disclosed herein may be used for self-test and self-repair of a memory comprising first and second arrays. According to this embodiment, the entirety of the memory is tested as a single addressable array, and rows in the first and second arrays that fail the test are detected. After the entire memory has been tested, failing rows from the first array are replaced with non-failing rows from the second array in a repair operation. The entirety of the memory is then retested as a single addressable array. During the retest, failing rows in the second array are ignored. If failing rows are detected in the repaired first array during the retest, a "fail" result is returned; otherwise, a "pass" result is returned. The first array represents the accessible portion of the memory and the second array the redundant portion. According to the method disclosed herein, testing of the memory is done during the first stage of a two-stage procedure, and retesting during the second stage. The repair operation consists of recording the addresses

of failing accessible rows in a repair table; associated with each of these addresses is the address of a non-failing redundant row. Using the repair table, the BISR dynamically substitutes a good redundant row for every failing accessible row.

Brief Summary Text (18):
In addition to the above-mentioned improved BIST/BISR method and computer-usable medium, a system for self-test and self-repair of a semiconductor memory is contemplated herein. In an embodiment, the system consists of a first m.times.n memory array, a second p.times.n memory array, a single built-in self-test (BIST) engine adapted to test the first and second arrays as a single joint array and detect rows failing the test, and built-in self-repair (BISR) circuitry that replaces failing rows in the first array with non-failing rows from the second array. The BIST is configured to generate row addresses that span the entire memory array (i.e., m+p rows). The BISR circuitry is capable of assigning addresses generated by the BIST that exceed the dimensions of the first array (i.e., >m) to rows in the second array. The BISR circuitry may also be capable of reassigning the addresses of failing rows in the first array to rows in the second array. The BIST may test the memory array in two test stages. In the first test stage, the addresses of rows that fail are recorded in a defect list. If there are enough non-failing rows in the second array at the end of the first test stage to replace all the failing rows from the first array, the memory is repaired and retested in a second stage. During the second stage, defects in the first array result in a "fail" test result, while defects in the second array are ignored. If there are no defects in the first array, a "pass" result is returned. Memory tests performed by the BIST may consist of writing a bit pattern to a portion of the memory, then reading back the contents and comparing them to the original bit pattern. A commonly used bit pattern, called a checkerboard, consists of alternating 1's and 0's.

Detailed Description Text (17):
In a second stage, the BIST may retest the memory, again generating row addresses from 0 to m+p-1. As it does so, the BISR monitors the addresses on mem_address bus 76. If an address is within the accessible memory (i.e., <m), the BISR compares it to the defective row addresses in its repair table. For each defective accessible row, the BISR substitutes the associated good redundant row. Thus, when the BIST retests the first m rows of the memory, it is actually testing a combination of accessible and redundant rows that tested good in the first stage. If an error occurs in the first m rows during the second stage, the memory is considered non-repairable, and the BISR toggles the externally-accessible FAIL flag 84. Addresses beyond the accessible memory (i.e., =m-1) are effectively omitted from testing. During the second stage, when the BISR detects an out-of-range address on mem_address bus 76, it suppresses the error flags ERRN 78 and FAIL 84. This is justifiable, since these addresses are not within the nominal address range of the memory device.

L18: Entry 1 of 4 File: USPT Jun 3, 2003

DOCUMENT-IDENTIFIER: US 6574757 B1
TITLE: Integrated circuit semiconductor device having built-in self-repair circuit for embedded memory and method for repairing the memory

Abstract Text (1):
An integrated circuit semiconductor device comprises a built-in self-repair (BISR) circuit including a plurality of row fill entries and a plurality of column fill entries for storing faulty memory cell information of an embedded memory. Sizes of the row and column fill entries are determined by the numbers of row and column redundancies of the embedded memory. The row/column fill entries store row/column addresses of the faulty memory cells, and the number of the faulty memory cells occurring at the same row/column address, respectively. In addition, the row/column fill entries include pointers for indicating opposite entries storing the column/row address corresponding to the row/column address. For repairing the faulty memory cells with the row and column redundancies, the BISR circuit selects row/column fill entries and deletes the number of the fault memory cells stored in the opposite fill entry. Thus, the information is deleted from the row/column fill entries with the exception of information to be repaired. Therefore, the self-repair of the faulty memory cells can be performed in the BISR circuit in response to the remaining information.

Brief Summary Text (2):
The present invention relates to a circuit and method for built-in self-test (BIST) and built-in self-repair (BISR) for a memory circuit in a semiconductor integrated circuit device.

Brief Summary Text (4):
Recently, core-based integrated circuit (IC) designs are drawing great attention, as the system-on-a-chip (SOC) design style gains momentum as a new design trend. Accordingly, a memory core or an analog core as well as a central processing unit (CPU) core are frequently used in the IC design. With the trend of SOC design, a complex circuit or system chip such as a CPU requires embedded memories of ever-higher capacity to improve system bandwidth.

Brief Summary Text (7):
To address this issue, the SOC commonly comprises a built-in self test (BIST) circuit for performing self-test, and a built-in self repair (BISR) circuit for performing self-repair. The BISR circuit includes a repair algorithm for determining whether the faulty memory cells are repairable or not, and for performing logical repair through software. As described above, the repair method of the BISR circuit is different from the external memory tester or the ATE performing physical repair. An embodiment of above described self-test and self-repair becomes an essential part in recent processor design techniques developing into the SOC. Examples of the BIST circuit and BISR circuit can be found in U.S. Pat. No. 5,920,515 to Shaik et al., issued on July 1999, REGISTER-BASED REDUNDANCY CIRCUIT AND METHOD FOR BUILT-IN SELF-REPAIR IN A SEMICONDUCTOR MEMORY DEVICE; and U.S. Pat. No. 5,987,632 to Irrinki et al., issued on November 1999, METHOD OF TESTING MEMORY OPERATIONS EMPLOYING SELF-REPAIR CIRCUITRY AND PERMANENTLY DISABLING MEMORY LOCATIONS.

Brief Summary Text (9):
For this reason, some SOCs embedding the BISR circuit restrict the limits to be repaired. For example, the numbers of the row and column redundancies are restricted to within 1, respectively. In case that the respective redundancies are one or one pair, the structure of the BISR circuit becomes simple. In that case, the SOC has a restriction that the SOC can repair only one row and one column.

Brief Summary Text (12):
A novel BISR circuit and a repair method are therefore required to repair the faulty memory cells of an embedded memory having multiple redundancies, in a more precise manner.

Brief Summary Text (13):
It is therefore an object of the present invention to provide an integrated circuit semiconductor device having a BISR circuit for an embedded memory with multiple redundancies.

Brief Summary Text (14):
It is another object of the invention to provide a repair method of a BISR circuit for an embedded memory with multiple redundancies.

Brief Summary Text (22):
According to another aspect of this invention, there is provided a repair method of a BISR circuit for an embedded memory with multiple redundancies comprising the steps of: filling row/column information to first/second data storing means, respectively, wherein the row/column information include row/column addresses of faulty memory cells, the number of the faulty memory cells having the same row/column addresses, and entry location of opposite data storing means storing column/row addresses corresponding to the respective row/column addresses; determining repair methods of the faulty memory cells as much as the number of row or column redundancies by selecting entry composing the first or the second data storing means in order of the number of the faulty memory cells stored in the entry, and decreasing the number of the faulty memory cells stored in the entry location of the opposite data storing means appointed by the selected entry; and generating repaired addresses to the memory according to the determined repair methods.

Drawing Description Text (13):
FIG. 9 is a schematic flowchart for illustrating an operation of the BISR circuit shown FIG. 1;

Drawing Description Text (16):
FIG. 12 is a diagram for illustrating repair coverage of the BISR circuit using the row and column fill entries shown in FIGS. 3A and 3B, and the conventional fill entries shown in FIG. 2.

Detailed Description Text (3):
FIG. 1 is a block diagram illustrating an integrated circuit semiconductor device according to a preferred embodiment of the present invention. Referring to FIG. 1, the SOC system comprises an embedded memory 30, a BIST circuit 10 for testing the SOC system including the memory 30, and a BISR circuit 20 for repairing the SOC system in response to the tests result from the BIST circuit 10.

Detailed Description Text (5):
The BIST circuit 10 includes a BIST controller 11, an address generator 12, a data generator 13, and a comparator 14. The BISR circuit 20 includes a BISR controller 21, an address checker 22, a first fill logic 23, a second fill logic 24, row fill entries 25, column fill entries 26 and an allocation logic 27. The row and column fill entries 25 and 26 are internal memories comprising a plurality of entries for storing row and column faulty memory cell information occurred in the embedded

memory 30. In many cases, the row/column fill entries 25 or 26 are called a failure address memory (FAM). Test and repair operations of the BIST circuit 10 and the BISR circuit 20 for the embedded memory 30 are illustrated as follows.

Detailed Description Text (6):
The BIST controller 11 controls overall BIST operations according to its implemented test algorithms. The address generator 12 generates addresses Addr for transmission to the memory 30. Addresses Addr are composed of row addresses and column addresses. Data generator 13 generates input data Din to be compared with read-out data Dout. The comparator 14 compares the input data Din with the read-out data Dout, and generates faulty memory cell information to the BISR controller 21 of the BISR circuit 20 if there is a mismatch.

Detailed Description Text (7):
The BISR circuit 20 usually operates together with the BIST circuit 10. The BISR controller 21 controls overall BISR operation. It begins operation by receiving the faulty memory cell information from the BIST circuit 10. In a preferred embodiment, when the BISR circuit 20 is in operation, the BIST circuit 10 halts operation and waits pending completion of BISR operation.

Detailed Description Text (8):
When the BIST circuit 10 provides the faulty memory cell information for the BISR controller 21, the first and the second fill logic 23 and 24 store the addresses and the number of the failures to the row fill entries 25 and the column fill entries 26, respectively. The row fill entries 25 and the column fill entries 26 include pointers for appointing entry locations of the opposite entries 26 and 25, respectively, which will be described in detail later. By using the pointers, entry locations of the opposite entries 26 or 25 storing column/row addresses corresponding to the row/column addresses of the faulty memory cells can be verified. The respective pointers are stored by the allocation logic 27.

Detailed Description Text (9):
After storing the faulty memory cell information to the row and column fill entries 25 and 26, completely, the BISR controller 21 selects either the row fill entries 25 or the column fill entries 26. The selected entries have fewer entries compared to the unselected entries. In addition, the BISR controller 21 determines repair methods of the selected row or column fill entries by selecting respective entries in order of the stored number of the faulty memory cells. If the repair methods of the selected fill entries are determined completely, the same procedure is performed for the other fill entries 25 or 26, and vice versa.

Detailed Description Text (10):
When the entry is selected for determining the repair method, the allocation logic 27 decreases the number of the faulty memory cells by 1 stored in the opposite entry appointed by the selected entry, under control of the BIST controller 21. In that case, if the decreased number of the faulty memory cells is zero (i.e., 0), the corresponding entry is deleted by the allocation logic 27. After finishing determining repair methods of the faulty memory cells according to the above described process, the BISR circuit 20 generates and provides repaired addresses to the memory 30 in response to the addresses of the faulty memory cells.

Detailed Description Text (11):
According to the above-mentioned operation of the BISR circuit 20, the faulty memory cells can be repaired in the SOC itself by using the row/column redundancies of the memory 30. The repair method according to the present invention using the row and column entries 25 and 26 provides high repair recovery, regardless of the number of the row/column redundancies 31 or 32.

Detailed Description Text (12):
FIG. 2 is a diagram for illustrating a structure of conventional fill entries. The

conventional BISR circuit includes fill entries storing the row and column address information of the faulty memory cells. Generally, the number of the faulty memory cells is 2.times.R.times.C to be stored as address information in the fill entries, when the embedded memory includes R row redundancies and C column redundancies. Thus, the number of the fill entries is 2.times.R.times.C as shown in FIG. 2. In that case, since a repair algorithm is performed by the row and column addresses of the faulty memory cells stored in the same fill entries, the restrictions to perform the repair algorithm increase proportionally as the number of the faulty memory cells and the redundancies increase.

Detailed Description Text (13):
Referring to FIG. 2, the `Valid` field indicates the validity of information. The `Row Address` field is used for storing a row address of the faulty memory cell, and the `Row Hit Count` field is used for storing the number of the detected faulty memory cells which have the same row address. The `Column Address` field is used for storing a column address of the faulty memory cell, and the `Column Hit Count` field is used for storing the number of the detected faulty memory cells which have the same column address. In addition, the `Row/Column Must` field is set when a row/column is determined to require repair. In that case, it is a problem that the fault recovery of the conventional BISR circuit using the fill entries is decreased in proportion as the number of the faulty memory cells and the number of the row/column redundancies are increased.

Detailed Description Text (14):
Therefore, the BISR circuit 20 (see FIG. 1) according to the present invention constructs the row fill entries and the column fill entries, respectively, by splitting the faulty memory cell information into the row fill entry and the column fill entry to perform the self-repair. Hardware overhead is therefore reduced. In addition, the respective row and column entries store opposite fill entry information, so that the BISR circuit 20 can repair the faulty memory cells exactly, even though the row/column redundancies are increased. The structures of the row and column fill entries 25 and 26 are described as follows.

Detailed Description Text (33):
If the steps for storing information related to the faulty memory cells are repeated as shown in FIGS. 6C to 6J, the row and column fill entries 25 and 26 storing information of whole faulty memory cells can be obtained as shown in FIG. 6J. After completing storing faulty memory cell information to the row and column fill entries 25 and 26, the BISR circuit 20 according to the present invention determines repair methods of the faulty memory cells by using the stored information and repairs the faulty memory cells through the determined repair methods. The steps for determining repair method of the faulty memory cells according to the present invention are illustrated as follows.

Detailed Description Text (34):
FIGS. 7A-7F are diagrams for illustrating steps for determining repair methods of the faulty memory cells a-j shown in FIG. 5 according to the information stored in the row and column fill entries 25 and 26 shown in FIGS. 6A-6J. The BISR circuit 20 according to the present invention decreases the number of the faulty memory cells stored in opposite fill entries during determining the repair methods of the faulty memory cells a-j stored in row/column fill entries 25 or 26. After completing determination of the repair methods, the faulty memory cells a-j are repaired by the information stored in the row and column fill entries 25 and 26. After repairing, the BISR circuit 20 generates repaired addresses to the embedded memory 30.

Detailed Description Text (48):
For example, if the faulty memory cells are distributed symmetrically in every direction on the basis of a specific cell, the faulty memory cells are unrepairable. According to the present invention, these cells are determined

repairable or unrepairable by location of the cells. However, frequency in occurrence of such distribution of the faulty memory cells is very low. Thus, the BISR circuit according to the present invention and the repair method of the same can repair most faulty memory cells. In addition, the BISR circuit and the repair method have high repair coverage.

Detailed Description Text (50):
FIG. 9 is a flow diagram for illustrating an operation of the BISR circuit 20 shown in FIG. 1. Referring to FIG. 9, at step S20, the BISR circuit 20 according to the present invention stores faulty memory cell information to the row fill entries 25 and the column fill entries 26, respectively. At step S40, repair methods of respective entries are determined by selecting entry of the row fill entries 25 and the column fill entries 26 in order of repair efficiency, and the number of faults stored in the opposite fill entry corresponding to the selected entry is decreased by 1. Thus, information to be repaired can be remained in the row and column fill entries 25 and 26. In that case, the repair efficiency is increased when an entry storing a large number of faults is selected. Continually, at step S60, the BISR circuit 20 generates repaired addresses to the memory 30 through logical repair of the faulty memory cells.

Detailed Description Text (57):
FIG. 12 shows experimental results of repair coverage of the BISR circuit. Referring to FIG. 12, `A` and `B` are graphs for illustrating repair coverage of the BISR circuit using the row and column fill entries 25 and 26 shown in FIGS. 3A and 3B, and using the conventional fill entries shown in FIG. 2, respectively. The X-axis represents the number of faults injected in a sparse array. The Y-axis represents the repair coverage. The graphs illustrate experimental results when the numbers of row and column redundancies of the embedded memory 30 are 3 and 2, respectively. To obtain the results shown in FIG. 12, ten million simulations are performed in each number of the faults (for example, 6 to 12), so that the number of simulations totaled to seventy million.

Detailed Description Text (58):
The simulations are performed in case that the number of the faults is 6 to 12. If the number of the faults is 5, the 5 faults can be repaired under any methods, sufficiently, since the sum of the row and column redundancies is 5. Thus, the simulations begin when the number of the faults is 6. In addition, when the numbers of row and column redundancies of the embedded memory 30 are 3 and 2 respectively, the BISR circuit according to the present invention and any BISR circuit according to the conventional method can not repair more than 2.times.R.times.C faults (i.e., 2.times.3.times.2=12). Thus, the repair coverage exceeding 12 faults is not considered.

Detailed Description Text (62):
Therefore, the BISR circuit according to the present invention can maintain almost constant repair coverage, although the number of the redundancies and the number of the faults are increased. Thus, the BISR circuit can repair the faulty memory cells occurred in the embedded memory with multiple redundancies, more exactly.

L2: Entry 2 of 11 File: USPT Jan 7, 2003

DOCUMENT-IDENTIFIER: US 6505313 B1
TITLE: Multi-condition BISR test mode for memories with redundancy

Abstract Text (1):
A memory device configured to detect changes in fault patterns is disclosed. In one embodiment, the memory device includes a memory array, a built-in self-test (BIST) unit, and a built-in self-repair (BISR) unit. The BIST unit runs test patterns on the memory array to identify faulty locations in the array. A comparator within the BIST or external to the BIST compares the actual output of the memory array to the expected output, and asserts an error signal whenever a mismatch occurs. The BISR unit intercepts addresses directed to the memory array, and operates on the addresses in three distinct phases. During a training phase, the BISR unit stores the intercepted addresses when the error signal is asserted. During the normal operation phase, the BISR unit compares all intercepted addresses to stored addresses and redirects a corresponding memory access if any intercepted address matches a stored address. During a verification phase, the BISR unit compares intercepted addresses designated by assertions of the error signal to the addresses previously stored in the training phase. If the faulty intercepted address fails to match a stored address, the BISR unit asserts a "new error" signal. If at the end of the verification phase, a stored address has not matched nay intercepted faulty address, the BISR asserts a "missed error" signal.

Brief Summary Text (8):
To reduce repair costs and allow field repairs, some memory chips have been equipped with built-in self test (BIST) and built-in self repair (BISR) circuitry. The BIST circuit detects faults in the memory array and notifies the BISR circuit of the fault locations. The BISR circuitry generally reassigns the row or column containing the failing cell to a spare row or column in the memory array. BIST and BISR are typically performed each time power is applied to the system. This allows any latent failures that occur between subsequent system power-ups to be detected in the field.

Brief Summary Text (9):
Occasionally, the faults that occur in a memory chip are condition-sensitive. For example, some faulty cells may operate normally at power-up, but cease functioning under normal operating conditions. Other faults may be sensitive to the power supply voltage level. While BIST and BISR circuitry can compensate for these problems, changes in fault patterns of a chip are undesirable and may be symptomatic of underlying manufacturing problems. Consequently, it is desirable to provide a method of screening chips at the factory to detect fault pattern changes.

Brief Summary Text (11):
Accordingly, there is disclosed herein a memory device configured to detect changes in fault patterns. In one embodiment, the memory device includes a memory array, a built-in selftest (BIST) unit, and a built-in self-repair (BISR) unit. The BIST unit runs test patterns on the memory array to identify faulty locations in the array. A comparator within the BIST or external to the BIST compares the actual output of the memory array to the expected output, and asserts an error signal whenever a mismatch occurs. The BISR unit intercepts addresses directed to the

memory array, and operates on the addresses in three distinct phases. During a training phase, the BISR unit stores the intercepted addresses when the error signal is asserted. During the normal operation phase, the BISR unit compares all intercepted addresses to stored addresses and redirects a corresponding memory access if any intercepted address matches a stored address. During a verification phase, the BISR unit compares intercepted addresses designated by assertions of the error signal to the addresses previously stored in the training phase. If the faulty intercepted address fails to match a stored address, the BISR unit asserts a "new error" signal. If at the end of the verification phase, a stored address has not matched any intercepted faulty address, the BISR asserts a "missed error" signal.

Drawing Description Text (3):
FIG. 1 depicts a functional block diagram of a memory equipped with BIST and BISR according to one embodiment;

Drawing Description Text (4):
FIG. 2 depicts a functional schematic diagram of a first BISR embodiment that detects changes in fault patterns;

Drawing Description Text (6):
FIG. 4 depicts a functional block diagram of a BISR component for detecting changes in fault patterns.

Detailed Description Text (2):
In the following description, the terms "assert" and "de-assert" are used when discussing logic signals. When a logic signal is said to be asserted, this indicates that an active-high signal is driven high, whereas an active-low signal is driven low. Conversely, de-assertion indicates that an active-high signal is driven low, and that an active-low signal is driven high. As used herein, the term "BIST" refers to the actual test, while "BIST unit" and "BIST circuitry" refer to the circuitry that performs BIST. Similarly, "BISR" refers to the process of built-in self repair, while "BISR unit" and "BISR circuitry" refer to the circuitry that performs BISR.

Detailed Description Text (4):
Turning now to the figures, FIG. 1 shows a memory 100 having a set of signal lines that includes an address bus (ADDR), a read/write line (R/W), a bi-directional data bus (DATA), a test mode bus (TMODE), and a fail line (FAIL). A set of multiplexers 104, 106, and 108 allows a BIST unit 110 to take control of the ADDR, R/W, and DATA lines, respectively, when the TMODE bus includes an asserted test signal. The ADDR lines from multiplexer 104 connect to BISR circuit 112, and from there to an address decoder in memory array 118. When provided with an address, the address decoder asserts a word line to access cells in memory cell array 118 that correspond to the value on the address lines. If the R/W line is asserted, the data from the accessed cells is driven onto the DATA lines. Otherwise, the binary values on the DATA lines are stored into the accessed cells.

Detailed Description Text (5):
BISR circuit 112 is provided to detect and block addresses of faulty cells, and to assert a replacement word line to access redundant cells to replace the faulty cells in the memory cell array. The BISR 112 circuit is preferably also configured to detect changes in fault patterns. The BISR circuit 112 may be considered as an undivided unit 112 or as a memory unit 116 and a remapping unit 114. In one embodiment of the invention is shown in terms of an undivided BISR unit 112, and a second embodiment is shown in terms of memory unit 116. Both embodiments are discussed further below.

Detailed Description Text (7):
Referring momentarily to FIG. 2, the BISR unit 112 includes a counter 202 which

increments an error count every time the ERR line is asserted. Counter 202 also produces an overflow signal (OVFL) that is asserted when the number of detected errors exceeds the number of redundant memory words available. Upon detecting assertion of the OVFL signal, BIST unit 110 (FIG. 1) ceases testing and holds the FAIL line in an asserted state. If the testing completes without assertion of the OVFL signal, BIST unit 110 de-asserts the FAIL line.

Detailed Description Text (10):
The phase of operation in which the BIST locates faults and configures the BISR to remap the faulty addresses to redundant memory locations is hereafter referred to as the training phase of the BISR unit. At some point subsequent to the training phase, the BIST unit will conduct a fault pattern verification test. In the fault pattern verification test, the BIST unit 110 will repeat its actions of the training phase. However, the BISR unit 112 retains some memory of the faults detected in the training phase, and compares them the faults detected by the BIST unit 110 in the fault pattern verification phase. Any difference between the sets of detected faults is identified by the BISR unit 112.

Detailed Description Text (11):
Referring now to FIG. 2, BISR unit 112 receives address bus ADDR, test mode signal (MODE.backslash.), error signal ERR, and remap signal REMAP. The MODE.backslash. signal is active low, and is asserted low during the verification phase to verify fault pattern consistency. The remainder of the time (during the training phase and during normal operation), the MODE.backslash. signal is de-asserted (high) to allow training of the BISR circuit and remapping by the BISR circuit. During training, the BISR circuit stores the addresses of detected fault locations. The BIST unit asserts the ERR signal during detection of a faulty address, and REMAP signal is asserted to cause the repair circuit 112 to remap those faulty addresses it has stored. In response to these signals, the BISR circuit provides a filtered address bus FADDR, redundant word line signals RWLx, a new error detect signal (ERRNEW), and a missing error detect signal (ERRMISS). The BISR circuit either passes the ADDR bus value on to the FADDR bus, or the BISR circuit blocks the value if the value matches a stored faulty address and asserts one of the RWLx signals to replace the faulty location. The ERRNEW signal is asserted if a new, unlatched error is found, and the ERRMISS signal is asserted if one or more previously latched errors are not found by a subsequent BIST.

Detailed Description Text (13):
Each of the stages can be understood in terms of four functional blocks: storage block 210, comparison block 220, filter block 230, and tracking block 240. Storage block 210 includes logical AND gate 211, address latch 213, and status latch 215. Logical AND gate 211 receives the MODE.backslash. signal, the ERR signal, and a signal from decoder 204. If all three are high, i.e. the BISR is being trained, an error is detected, and the decoder 204 is asserting the signal line for the current stage, the logical AND gate 211 provides a clock transition to address latch 213 and status latch 215. The address latch 213 stores the value on address bus ADDR, and the status latch 215 goes high to indicate that an address has been latched in the current stage.

Detailed Description Text (14):
Comparison block 220 includes logical AND gate 221, inverter 223, P-type transistor 225, N-type transistor 227, and inverted XOR gate 229. Logical AND gate 221 receives the REMAP signal, the output of the status latch 215, and an inverted blocking signal from a preceding stage. If all three are asserted, i.e. BISR remapping is enabled, an address is latched, and the preceding stage is not blocking the ADDR bus, then gate 221 asserts a switch signal.

Detailed Description Text (19):
Moving now the second embodiment, FIG. 3 shows a modular element of a BISR circuit memory module 116. The element 302 is configured to store faulty address locations

and compare the stored faulty addresses with newly-detected faulty addresses. Element 302 includes a multiplexer 304, an address latch 306, a reserve latch 308, and a compare gate 310. Multiplexer 304 receives a output signal from the reserve latch, an input signal (IN), and an input select signal (ISEL). The output of the multiplexer 304 is provided as an input (D) to address latch 306. Address latch 306 also receives a shift input signal (TI), a shift enable signal (TE), a clock signal (CLK), and a reset signal (RESET). When the shift enable signal (TE) and the reset signal (RESET) are de-asserted, a clock pulse causes the address latch 306 to store the value of the input signal (D) and provide it as output signal (OUT). When the shift enable signal (TE) is asserted and the reset signal is de-asserted, a clock pulse causes the address latch to store the value of the shift input signal (TI). Assertion of the reset signal causes the output signal to be reset low.

Detailed Description Text (24):
Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. For example, while the description is directed to memory arrays, the BIST and BISR units are readily adaptable to other reconfigurable electronic systems having redundant portions. It is intended that the following claims be interpreted to embrace all such variations and modifications.

CLAIMS:

1. A device which comprises: a reconfigurable component having redundant portions; a built-in self-test (BIST) unit coupled to the reconfigurable component and configured to test the reconfigurable component to identify faulty portions of the reconfigurable component; and a built-in self-repair (BISR) unit configured to store identifiers of the faulty portions and coupled to the reconfigurable component to configure the redundant portions to operate in lieu of the faulty portions, wherein the BIST unit is further configured to retest the reconfigurable component anew to identify faulty portions of the reconfigurable component at a subsequent time, wherein the BISR unit is further configured to receive subsequent identifiers of the faulty portions, and wherein the BISR unit is configured to compare the subsequent identifiers to the stored identifiers to identify any discrepancies; wherein said subsequent identifiers are stored by the BISR unit in a shift chain, and wherein the BISR unit is configurable to serially shift the contents of the shift chain to one or more external pins for off-chip examination; and wherein the stored identifiers are addresses stored in reserve latches, and wherein the subsequent identifiers are addresses stored in address latches, and the BISR unit includes logical XOR gates that perform bit-wise comparisons between the contents of the reserve and address latches to provide corresponding match signals to a detector that detects simultaneous assertion of all said match signals.

2. The device of claim 1, wherein the BISR unit is configured to assert a signal to indicate whether a discrepancy exists between the stored identifiers and the subsequent identifiers.

3. A memory device which comprises: a memory array; a BIST unit coupled to said memory array and configured to test said memory array to identify faulty locations in said array, wherein said faults are identified by assertion of an error signal; and a BISR unit coupled to said memory array and configured to intercept addresses directed to said memory array, wherein during a training phase, the BISR unit is configured to store the intercepted addresses when the error signal is asserted, wherein during normal operation, the BISR unit is configured to compare all intercepted addresses to stored addresses to redirect a corresponding memory access if any intercepted address matches a stored address, and wherein during a verification phase, the BISR unit is configured to compare intercepted addresses designated by assertions of the error signal to addresses stored in the training phase; wherein the BISR unit comprises: a counter coupled to receive the error signal and configured to increment an error count only when the error signal is

asserted; a decoder coupled to the counter to receive the error count, and configured to assert a decoder signal line that corresponds to the error count; one or more redundant location stages each coupled to receive the error signal and a corresponding decoder signal line; and a logic gate coupled to each of the stages and configured to assert a "new error" signal if none of said stages indicates a match between an intercepted address and a stored address during assertion of the error signal in the verification phase.

L2: Entry 1 of 11 File: USPT Nov 18, 2003

DOCUMENT-IDENTIFIER: US 6651202 B1
TITLE: Built-in self repair circuitry utilizing permanent record of defects

Abstract Text (1):
An integrated circuit includes built-in self test (BIST) and built-in self repair (BISR) circuitry, a fuse array capable of storing information related to defective memory locations identified during the manufacturing process. During manufacture, the integrity of the embedded memory of the integrated circuit is tested under a variety of operating conditions via the BIST/BISR circuitry. The repair solutions derived from these tests are stored and compiled in automated test equipment. If the repair solutions indicate that the embedded memory is repairable, the on-chip fuse array of the integrated circuit is programmed with information indicative of all of the detected defective memory locations. The built-in self repair circuitry of the integrated circuit is not executed upon power up. Instead, the repair information stored in the fuse array is provided to address remap circuitry within the BISR circuit. When an access to one of these memory locations is attempted during normal operation of the integrated circuit, the BISR circuitry remaps the memory operation to a redundant memory element.

Brief Summary Text (15):
In addition to the aforementioned testing procedures, manufacturers use a number of techniques to repair faulty memories when feasible. Such techniques include bypassing defective cells using laser procedures and fused links that cause address redirection. However, such techniques are limited to one-time repair and require significant capital investment. Further, these techniques may leave integrated circuits useless if the repaired memories become defective after shipment from the manufacturing site--even where test equipment is available to end users, traditional field repairs have been expensive, time consuming, and largely impracticable.

Brief Summary Text (16):
In order to enhance the repair process, on-chip built-in self repair (BISR) circuitry for repairing faulty memory cells has evolved. BISR circuitry functions internal to the integrated circuit without detailed interaction with external test or repair equipment. In the typical BISR approach, suitable test algorithms developed and implemented in BIST or BIST-like circuitry. These test patterns may be capable of detecting stuck-at, stuck-open, bridging faults and retention faults during memory tests. Following execution of the test patterns, the BISR circuitry analyzes the BIST "signature" (results) and, in the event of detected faults, automatically reconfigures the defective memory utilizing redundant memory elements to replace the defective ones. A memory incorporating BISR is therefore defect-tolerant. The assignee of the present invention, LSI Logic Corporation, has addressed different methods of repairing faulty memory locations utilizing BIST and BISR circuitry, as disclosed in U.S. Pat. No. 5,764,878, entitled "BUILT-IN SELF REPAIR SYSTEM FOR EMBEDDED MEMORIES", U.S. patent application No. 09/209,938, entitled "REDUNDANCY ANALYSIS FOR EMBEDDED MEMORIES WITH BUILT-IN SELF TEST AND BUILT-IN SELF REPAIR" filed Dec. 11, 1998, now U.S. Pat. No. 6,067262, and U.S. patent application No. 09/209,996, entitled "TESTING SCHEME FOR EMBEDDED MEMORIES USING BISR AND FUSE ID" filed Dec. 11, 1998, now U.S. Pat. No. 6,367,042, all of which are hereby incorporated by reference as if set forth in their entirety.

Brief Summary Text (17):
BISR compliments BIST because it takes advantage of on-chip processing capabilities to re-route bad memory bits rather than using an expensive and slow laser burning process to replace faulty memory locations. Some BISR circuitry is capable of repairing the faulty memory locations by redirecting the original address locations of faulty memory lines to the mapped addressed locations of the redundant columns and rows. Options for repair include either row and column replacement when a bad bit is found in a particular row or column.

Brief Summary Text (19):
With embedded memories, current BIST methodologies may not adequately detect memory locations having faults that are dependent on operating conditions (e.g., normal variations in voltage, timing, power supply disturbances and temperature). Even with BIST/BISR, memory elements can pass the power-up BIST under an initial set of operating conditions, only to fail during normal operation when the die is subsequently subjected to another set of operating conditions. Further, since BISR structures have a limited number of redundant memory locations, a device may be repairable only under select operating conditions. The problem may be exacerbated by the rigors of the packaging process, which may give rise to failure mechanisms not present in a given integrated circuit before singulation. Since BIST/BISR is typically run only once during a power cycle, any memory locations that fail after power-up may not be repaired. Such failures may cause the chip to be unsuitable for its intended use. Additionally, the execution time and off-chip circuitry required by BIST circuitry may be undesirable for certain end products.

Brief Summary Text (22):
In the disclosed embodiment of the invention, an integrated circuit die of a semiconductor wafer is provided with BIST/BISR circuitry and an embedded memory or similar circuit. The integrated circuit also includes a fuse array or other none-volatile circuitry capable of storing address information for defective memory locations. During manufacture, the integrity of the embedded memory of each integrated circuit die is preferably tested under a variety of conditions (also referred to as stress factors) via the BIST/BISR circuitry. The results of these tests are stored and compiled in ATE. The results are also referred to as BIST signatures or memory repair solutions. If the repair solutions indicate that the embedded memory is repairable, the on-chip fuse array of the integrated circuit is programmed with information indicative of all of the detected defective memory locations. Programming of the fuse array may occur prior to or following singulation and packaging of the integrated circuit die.

Brief Summary Text (23):
Once packaged and incorporated within an end product, the built-in self repair circuitry of the integrated circuit die is not executed upon power up. Instead, the repair information stored in the fuse array is provided to address remap circuitry within the BISR circuit. The repair information represents faulty memory locations detected during the manufacturing testing process under a variety of operating conditions. When an access to one of these memory locations is attempted during normal operation of the integrated circuit, the BISR circuitry remaps the memory operation to a redundant memory element.

Drawing Description Text (3):
FIG. 1 is a schematic diagram of an integrated circuit incorporating BIST/BISR and identification circuitry capable of being utilized with the present invention;

Detailed Description Text (3):
The integrated circuit IC comprises a built-in self-test (BIST) state machine/controller 102 for controlling the various other components of the disclosed memory BIST system, a built-in self repair (BISR) circuit 110, and a memory array 100. In addition to the BIST state machine/controller 102, other

components of the BIST circuitry include an address generator 104, a data generator 106 and a comparator 108. The BIST circuitry functions to generate and execute test patterns for detecting column and row faults in the memory array 100.

Detailed Description Text (4):
The BISR circuitry 110 is coupled to the memory array 100 and operates in conjunction with the BISR circuitry to repair detected faults in the memory array 100. The repair process may be accomplished by any of a number of techniques, including redirecting the original address locations of faulty memory elements to the mapped address locations of redundancy elements. The BISR circuitry 110 of the disclosed embodiment comprises a fault latch and repair module 112 and a FLARESCAN register 114. The memory array 100 may be a dynamic random access memory (DRAM), a static random access memory (SRAM), a read-only memory (ROM), or any other type of circuitry having a structured array(s) of elements conducive to built-in self test and repair.

Detailed Description Text (10):
Similarly, the ADDRESS inputs of the memory array 100 are driven by the output(s) of the BIST address generator 104. The outputs of the BIST address generator 104 thereby control the address inputs of the memory array 100 during execution of a test pattern algorithm. Thus, the BIST address generator 104 and BIST data generator 106 may provide address and data sequences, respectively, to the memory array 100 in an order as specified by a test pattern algorithm. Preferably, such sequences provide a set of data bits in a pattern that maximizes fault coverage for detecting various types of faults within the memory array 100. A system clock signal SYSTEM_CLOCK is also provided to both the BIST state machine controller 102 and the BISR circuitry 110 for logic clocking and synchronization.

Detailed Description Text (11):
During testing, data patterns provided to the memory array 100 by the BIST circuitry are propagated through the memory array 100 to the output bus SYS_DATA_OUT. Under BIST operation, these outputs are routed to the comparator 108, which compares the outputs of the memory array 100 on a read cycle against the corresponding binary bits produced by the BIST data generator 106 on the initiating write cycle. In the disclosed embodiment of the invention, an error signal ERR driven by the output of the comparator 108 is provided to the fault latch and repair module of the BISR circuitry 110. If there is no difference between DATA_IN and DATA_OUT, the error signal ERR is not asserted. If there is a difference, the ERR signal is asserted to indicate that a fault has been detected at that particular memory location.

Detailed Description Text (12):
The error signal ERR is utilized by the BISR circuitry 110 to perform self repair operations on the memory array 100. More specifically, the fault latch and repair module 112 repairs defective memory locations by redirecting accesses to defective address locations to address locations which can retain valid data. To this end, a redundant memory location control signal REDUNDANCY CONTROL is provided from the fault latch and repair module 112 to the memory array 100, and is asserted as necessary to prevent access to faulty memory locations. The fault latch and repair module 112 monitors the output of the BIST address generator 104 to identify pending accesses to defective memory locations. As detailed below, such memory locations are identified by the fuse array 150 after the integrated circuit IC has been incorporated into an end product. The fault latch and repair module 112 also provides a pass/fail signal PASS/FAIL to other circuitry, which may include external test equipment or the BIST state machine controller 102.

Detailed Description Text (13):
In the disclosed embodiment, the addresses of faulty memory locations are provided from the fault latch and repair module 112 to a fault-latching and repair execution, or FLARESCAN, register 114. The contents of the FLARESCAN register 114

may then be scanned out to ATE via a register output signal FLARESCAN_OUT. Table 1 is an exemplary bit capture file retrieved from a FLARESCAN register 114 following execution of BIST/BISR procedures, and represents faulty memory locations of different integrated circuits IC of a single wafer (not separately illustrated). Data from subsequent BIST runs can be compared as described below to determine if additional memory locations fail under different stress factors. Further details of one such comparison process can also be found in the previously incorporated U.S. Patent Application entitled "REDUNDANCY ANALYSIS FOR EMBEDDED MEMORIES WITH BUILT-IN SELF TEST AND BUILT-IN SELF REPAIR."

Detailed Description Text (15):
The integrated circuit IC further includes BIST/BISR circuitry 122 such as that shown in FIG. 1. The BIST/BISR circuitry 122 interfaces with an embedded memory array 100 as previously described, and also communicates with the external ATE 160 via the register output FLARESCAN_OUT or similar means. The register output signal FLARESCAN_OUT provides the external ATE 200 with addresses of memory locations of the embedded memory array 100 which fail BIST analysis.

Detailed Description Text (16):
In the disclosed embodiment of the invention, clocking of the BIST/BISR circuitry 122 is controlled by a clock signal FLARESCAN_IN_CLK from the external ATE 160. Other control signals may also be communicated as necessary from the external ATE 160 to the BIST/BISR circuitry 122.

Detailed Description Text (20):
Referring now to FIGS. 3A and 3B, flowcharts of an exemplary procedure according to the present invention for programming a fuse array 150 are provided. Briefly, the procedure involves many potential stages, including execution of BIST/IBISR routines at at least one set of operating conditions or stress factors, followed by programming of the fuse array 150 with information indicative of resulting detected defective memory locations. The BIST/BISR routines may be executed prior to singulation of the integrated circuit IC from the semiconductor wafer and/or after the integrated circuit IC has been subjected to the rigors of the packaging process. As described in greater detail in conjunction with FIG. 4, the information stored within fuse array 150 is utilized by the BISR circuitry 110 to repair defective memory locations of the memory array 100 without the necessity of first performing a BISR procedure.

Detailed Description Text (21):
It should be understood that the term "stress factor" refers to one or more environmental or operating conditions, and may include varying combinations of factors, such as temperature and humidity, temperature and voltage, speed and voltage, etc. For example, temperature and voltage may be applied to the integrated circuit IC under minimum/maximum operating conditions. Typically, a BIST/BISR run is executed when the integrated circuit IC is subjected to minimum temperature and maximum voltage. In addition, a BIST/BISR run is normally executed when the integrated circuit IC is subjected to maximum temperature and minimum operating voltage. As will be appreciated by those skilled in the art, different failure mechanisms may be manifested under different operating conditions. Consequently, the integrated circuit IC is preferably subjected to a host of stress factors and is tested under various conditions to improve the reliability and accuracy of the information stored within the fuse array 150.

Detailed Description Text (22):
Beginning with FIG. 3A, the exemplary fuse array 150 programming procedure is described in greater detail. Following commencement of the programming procedure (step 200) for a given integrated circuit IC, the integrated circuit IC is exposed to an initial set of one or more stress factors in step 202. As an example, the integrated circuit IC may be subjected to a minimum temperature as specified in the data sheet of the device. A predetermined amount of time is preferably allowed to

elapse in order for the integrated circuit IC to adjust to the initial set of stress factors. Power is also applied to the integrated circuit IC at this stage. Next, an initial BIST/BISR routine is executed at step 204. In the disclosed embodiment of the invention, diagnosis of the integrated circuit IC by the BIST/BISR circuitry 122 is performed upon an initial power-up or when initiated by the external ATE 160. In conjunction with step 204, an initial set of faulty memory locations for the integrated circuit IC under test is developed in step 206. This initial set of faulty memory locations (e.g., the BIST signature), as well as any other desired information, is then retrieved and stored by the external ATE 160.

Detailed Description Text (23):
Next, one or more additional sets of stress factors are applied to the integrated circuit IC under test in optional step 208. For example, the integrated circuit IC may be subjected to a maximum of specified temperature and other stress factor such as a supply voltage variation. For each additional set of stress factors, an additional BIST/BISR routine is executed as depicted in step 210. For each such additional BIST/BISR routine, an additional set of faulty or defective memory locations is generated and stored in the ATE 160 as shown in step 212.

Detailed Description Text (25):
One skilled in the art will appreciate that programming of the fuse array 150 need not necessary be performed after all BIST/BISR runs, but could be performed after each run. Further, as previously noted, programming of the fuse array 150 could be accomplished via circuitry incorporated within the integrated circuit IC itself. In any event, the information programmed in the fuse array 150 can be subsequently utilized by the BIST/BISR circuitry 122 without first performing a BIST analysis.

Detailed Description Text (26):
It will also be appreciated that execution of the BIST/BISR routines in steps 204 and 210 may be performed both prior to and following singulation and packaging of the integrated circuit IC from the other die of the semiconductor wafer. The rigors of the assembly or packaging process may create new failure mechanisms for the singulated integrated circuit IC, and it is therefore desirable that at least one BIST/BISR routine be performed on the package part. In addition, the manufacturing and testing process may include a step referred to in the art as "burn-in". Burn-in generally refers to the process of exercising an integrated circuit IC at elevated voltage and temperature. This process accelerates failures normally manifested as "infant mortality" (the early portion of the bath tub curb at the which failures decline with exposure to time) in a semiconductor device. Execution of the BIST/BISR routines is preferably performed following the burn-in process such that any resulting memory defects may be represented in the fuse array 150.

Detailed Description Text (27):
Compiling the results of BIST/BISR routines under the various sets of stress factors, both pre- and post-packaging, improves the fault coverage of the manufacturing test process. By analyzing the memory array 100 under various test conditions, and providing the compiled results to the fuse array 150, all faulty memory locations are repaired at the same time--even if the failure mechanisms are dependent on operating conditions.

Detailed Description Text (29):
Next, in step 306, the defective memory location information programmed into the fuse array 150 is provided to remap circuitry within the BIST/BISR circuitry 122. This information is used to repair faulty memory locations in much the same way that the results of a BIST run are used by traditional BISR circuitry. To this end, the BIST/BISR circuitry 122 monitors memory accesses to identify attempts to access defective memory locations as shown in step 308. If an access is not directed to a faulty memory location, normal memory access is permitted. If a defective memory location is addressed as determined in step 308 (vis-a-vis the information provided by the fuse array 150), the memory access is redirected to a specified redundant

memory element as shown in step 310. Subsequent memory accesses are handled in the same manner.

Detailed Description Text (30):
Thus, a method has been described for performing built-in self repair operations in an integrated circuit without first performing a built-in self test procedure. In the disclosed embodiment of the invention, the integrated circuit is provided with a fuse array or other non-volatile memory device which is programmed with information related to defective memory locations identified during the manufacturing process. During use of the integrated circuit in an end product, this information is directly used by BISR circuitry to remap address accesses from faulty memory locations to redundant memory elements. The need to execute a BIST routine each time power is supplied to the integrated circuit is thereby obviated. Further, because the stored fault information reflects test data gathered at a variety of operating conditions, the built-in self repair circuitry is capable of providing a higher degree of fault coverage than traditional BIST methods.

L7: Entry 5 of 36 File: USPT Feb 10, 2004

DOCUMENT-IDENTIFIER: US 6691247 B2
TITLE: Circuit and method for masking a dormant memory cell

Brief Summary Text (5):
One problem is that after such testing and repair of the matrix array, the redundant array often cannot be tested, and the matrix array often cannot be tested without implementing the repair solution. Such "back-end" tests (i.e., tests performed after repair of the matrix array) require a tester that has the capability to determine and store the addresses of the defective matrix cells during matrix-array testing and the unused redundant cells during redundant-array testing and to ignore errors that occur when these dormant cells are accessed. Unfortunately, due to its high cost, such a tester is usually reserved for the initial testing and repair described above, and a much cheaper back-end tester is used to test the matrix array after repair. Although such a back-end tester can test the matrix array with the repair solution enabled, it typically cannot test the matrix array with the repair solution disabled, or test the redundant array after the matrix array has been repaired. Therefore, such back-end testing of the matrix and redundant arrays is rarely, if ever performed.

Brief Summary Text (10):
One way to leakage test the entire array 10 after it has been repaired and without calculating a new data topo is to disable the repair solution so that all of the rows, even the defective matrix rows R and the unused redundant rows RR, are accessible to the tester. Although this would allow the tester to use the original data topo, the tester would have to calculate and store the repair solution so that it could avoid reading the defective matrix rows or unused redundant rows, or so that if the tester did read these dormant rows, it could ignore errors from these rows. (Although an unused redundant row may not include any defective cells 14, it may be disabled such that the cells 14 cannot be accessed.) If the tester did not do this, then it would falsely indicate that the part under test is defective, when in fact these defects are already mapped out by the repair solution. But as discussed above, a back-end tester typically cannot calculate and store a repair solution, and a tester that is relatively expensive and thus reserved for initial testing and repair. Furthermore, to increase back-end testing throughput, it is often desirable to test multiple circuits in parallel. Therefore, even if the tester could store a repair solution, it would have to store a different repair solution for each of the circuits. Unfortunately, even the most sophisticated testers often lack the ability to store multiple repair solutions. And even if a tester could store multiple repair solutions, the time required to calculate and store the repair solution for each circuit would be very time consuming, and thus would considerably slow down the testing throughput.